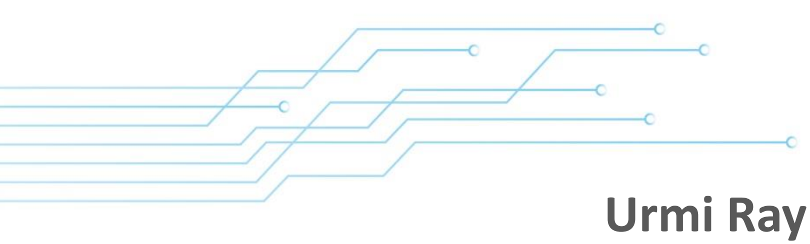
LEADING PROVIDER OF ADVANCED SEMICONDUCTOR PACKAGING
AND TEST SERVICES FOR GLOBAL CUSTOMERS

High Density Packaging Needs for Next Generation Connected Markets

2018.05.31



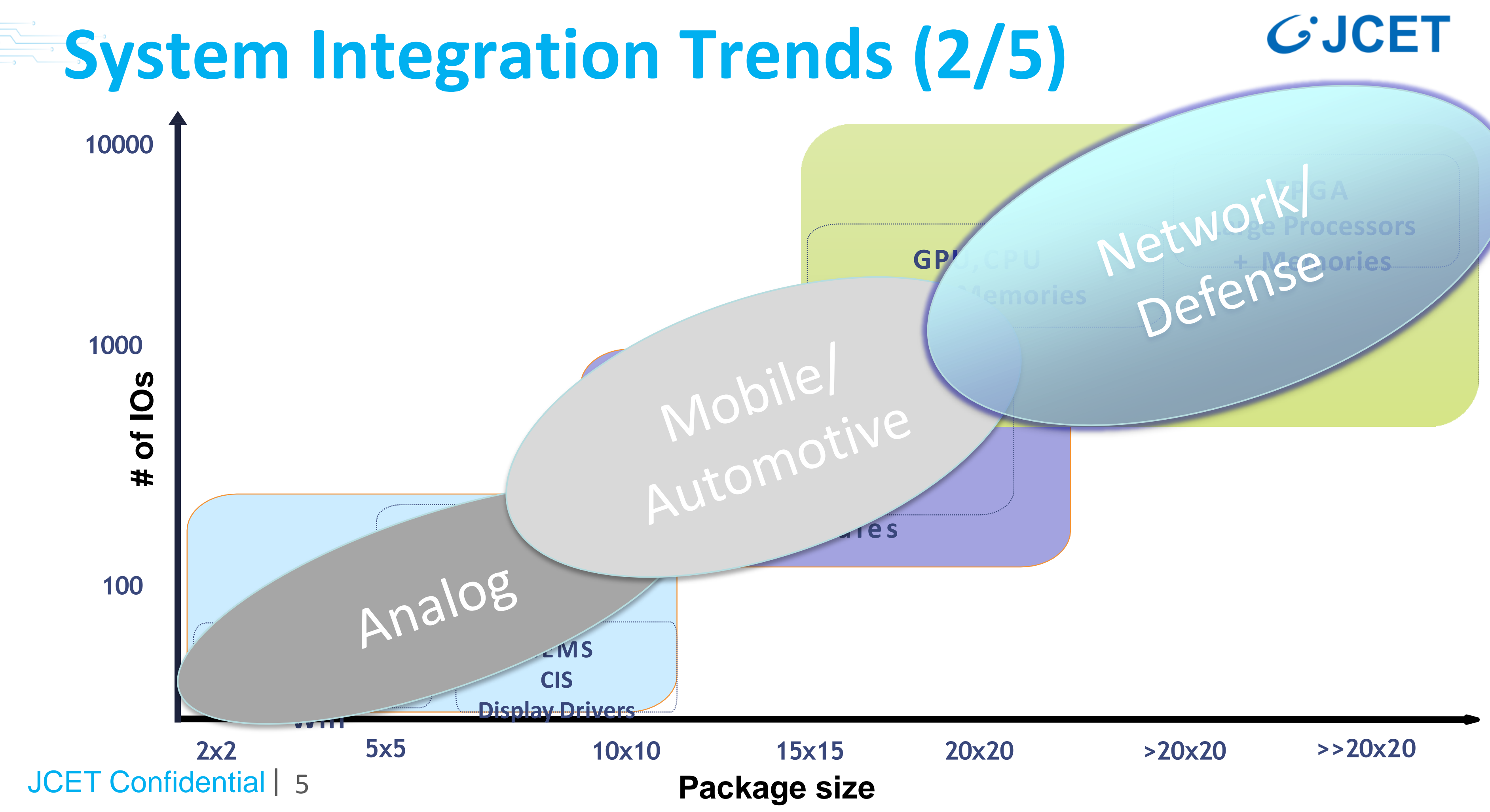
Urmi Ray

Contents

- Industry Advanced Packaging
  - System integration and COO optimization
- eWLB as high density packaging platform
- Conclusion

System Integration Trends (1/5)

# of IOs	Package size	Applications
~10–100	2x2 – 5x5	Analog, Wifi
~10–100	5x5 – 10x10	MEMS, CIS, Display Drivers
~100–300	5x5 – 10x10	BB, PMIC, RF/RFFEM
~100–1000	10x10 – 20x20	Application Processors, AP+BB, AP+DRAM, 5G Modules
~1000–10000	15x15 – >20x20	GPU,CPU, CPU + Memories
~1000–10000	>20x20 – >>20x20	FPGA, HPC Processors + Memories


System Integration Trends (2/5)
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10000
1000
100
# of IOs
Network/
Defense
Mobile/
Automotive
Analog
CIS
Display Drivers
2x2
5x5
10x10
15x15
20x20
>20x20
>>20x20
Package size
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System Integration Trends (3/5)

HIGH END

FPGA
Large Processors
+ Memories

GPU,CPU
CPU + Memories

MIDDLE END

Migration from QFN->WLP
Multi –die SIP
FOWLP
Low cost substrates & MIS

Application Processors
AP+BB
AP+DRAM

LOW END

QFN, P
WLCSP
FC-MIS
FOWLP
Multi-die FOWLP
Single side RFFEM

# of IOs: 10000, 1000, 100

Package size: 2x2, 5x5, 10x10, 15x15, 20x20, >20x20, >>20x20

System Integration Trends (4/5)

- Higher density interposer -POP
- POP Module subsystem
- Double sided RFFEM
- Effective memory integration
- Antenna in package for 5G

# of IOs: 10000, 1000, 100

Package size: 2x2, 5x5, 10x10, 15x15, 20x20, >20x20, >>20x20

MLP, Interposer POP

FOWLP-POP

POP Module Subsystem

Double side RFFEM

5G Module with antenna in package

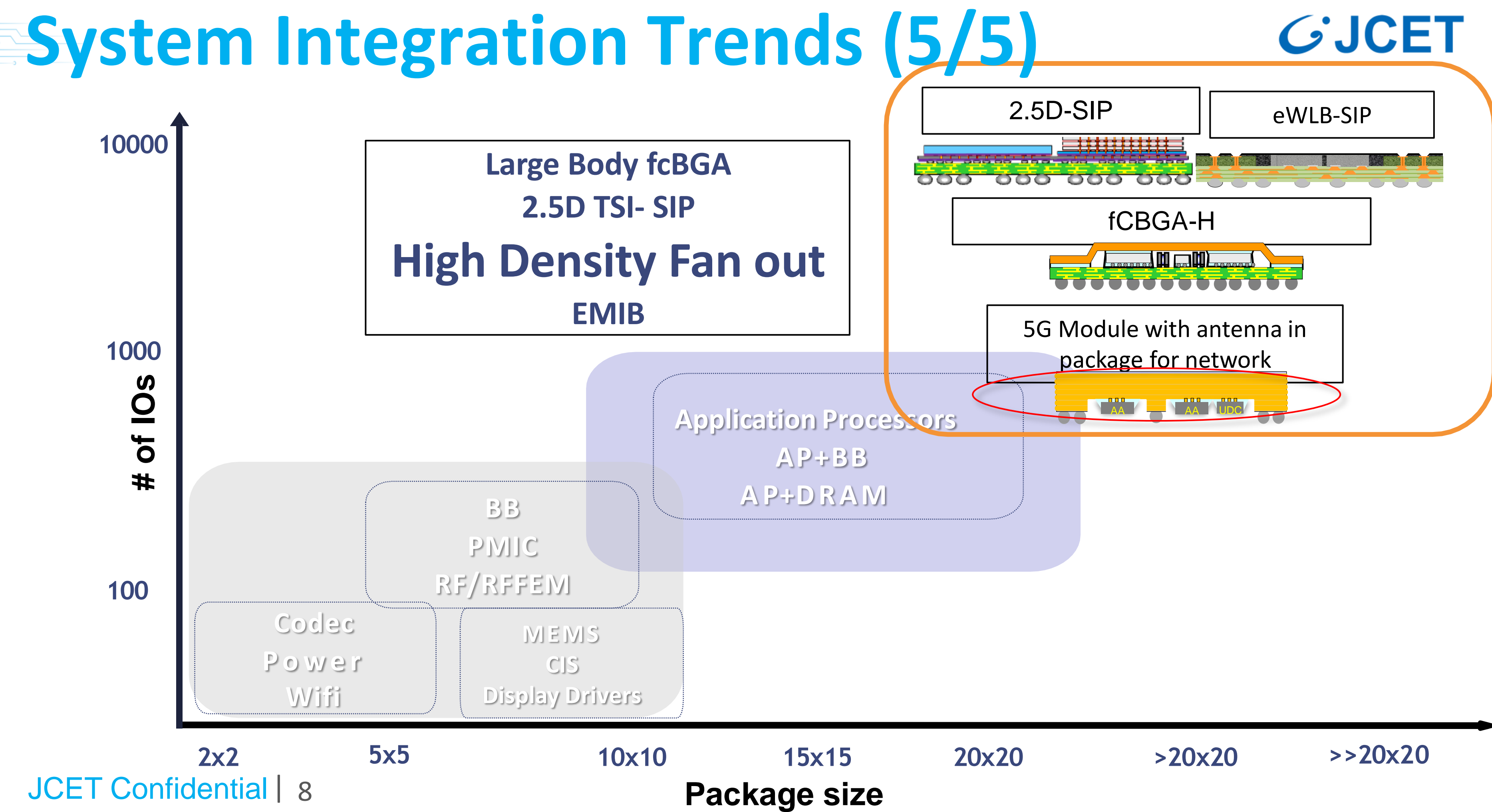
GPU, CPU
CPU + Memories

FPGA
Large Processors
+ Memories

BB
PMIC
RF/RFFEM

Codec
Power
Wifi

MEMS
CIS
Display Drivers



System Integration Trends (5/5)
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2.5D-SIP
eWLB-SIP
fCBGA-H
5G Module with antenna in package for network
AA
AA
UDC
Large Body fcBGA
2.5D TSI- SIP
High Density Fan out
EMIB
# of IOs
10000
1000
100
Application Processors
AP+BB
AP+DRAM
BB
PMIC
RF/RFFEM
Codec
Power
Wifi
MEMS
CIS
Display Drivers
2x2
5x5
10x10
15x15
20x20
>20x20
>>20x20
Package size

Packaging Technology Towards 4G+/5G

eWLB - high density packaging platform

High Density eWLB Package

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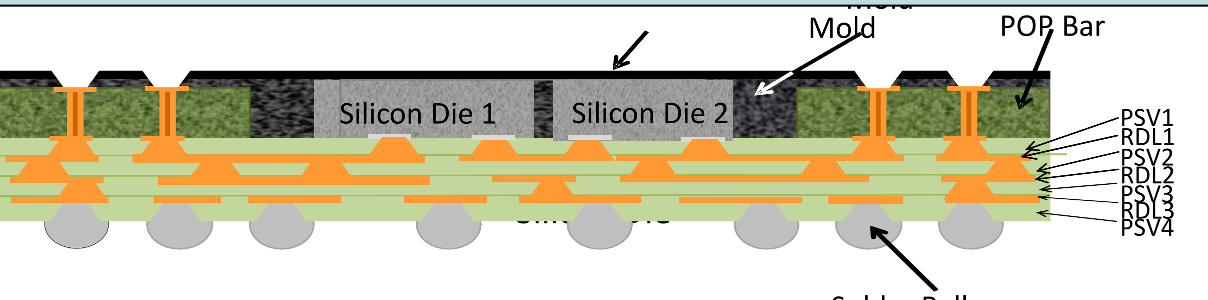
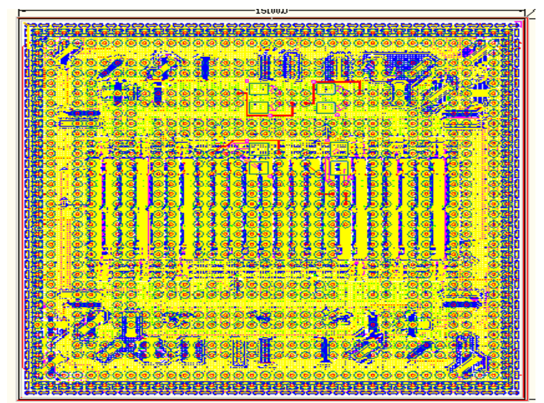
eWLB and Fan out packages can serve as means of high density packaging
An Example is shown here





Package Configuration (3L RDL)	
Die Size	11.16 x 5.58 mm & 11.16 x 5.58 mm
PKG Size	15x15mm
Ball Composition	SAC305
Ball Pitch (Bottom / Top)	400um / 200um
Die Thickness (min)	200um
RDL Stack Thickness (nominal)	39um
Package ball height/size	185um
PKG Total Thickness (nominal)	424um

RDL Stack	39um+/-10um
PSV1	4um +/- 1.0um
RDL1	3um +/- 1.0um
PSV2	5um +/- 1.0um
RDL2	4um +/- 1.0um
PSV3	6um +/- 1.5um
RDL3	8um +/- 1.5um
PSV4	9um +/- 1.5um
Bump Height (SAC305)	185um

Technology: Fine Pitch RDL1 – Litho, Plating and etching

Fine Pitch RDL Development successfully completed

RDL1 Litho (2um L/S)	RDL1 after Plating/Etch
• BTM CD ~ 2.03um • Sidewall Angle ~ 85º	• RDL1 thickness ~ 2.82 um • BTM CD ~ 2.34um • Sidewall Angle ≥ 85º • No undercut

Technology: RDL2

RDL2 Litho (5um L/S)	RDL2 after Plating/Etch
• BTM CD ~ 5.2um • Sidewall Angle ≥ 85º	• RDL thickness ~ 4.1 um • BTM CD ~ 5.0um • Sidewall Angle ≥ 85º • No undercut

Technology: 3L RDL – PSV Via Stack and RDL Stack

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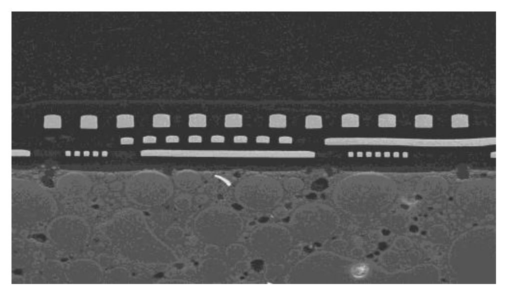
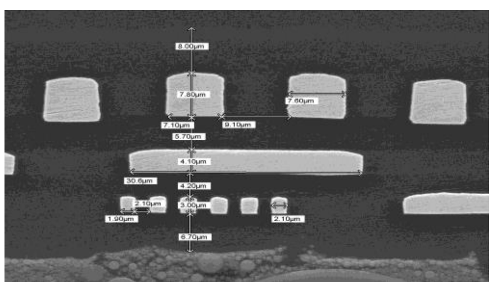
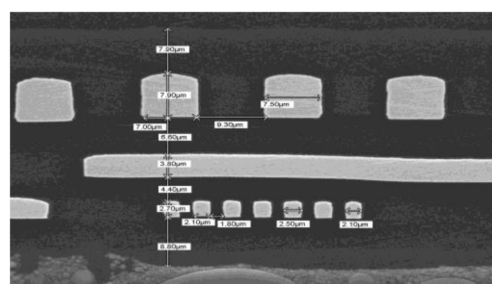
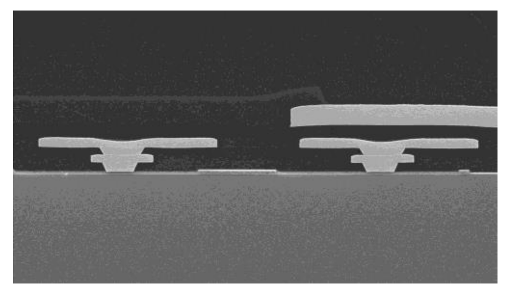
- **3L RDL Stack**

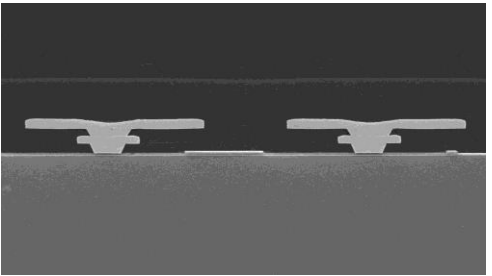


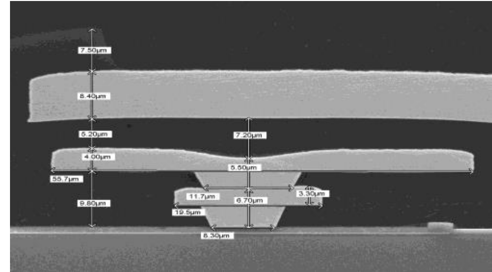




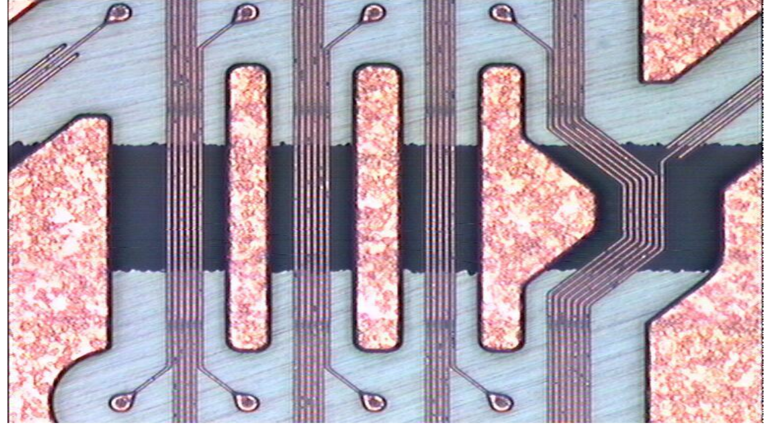
- **Stacked Via**

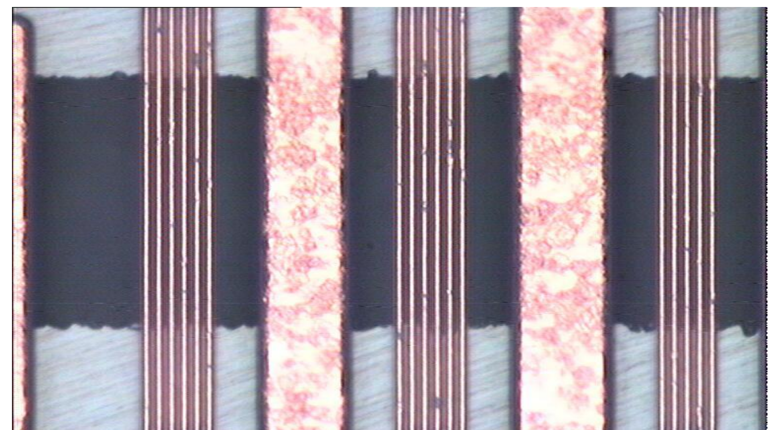


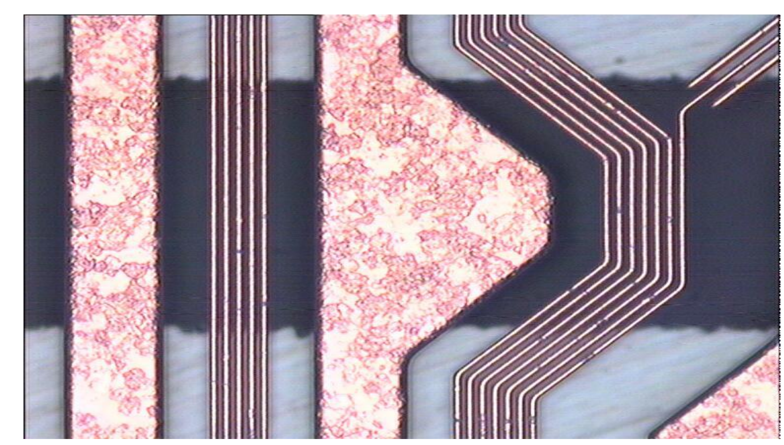




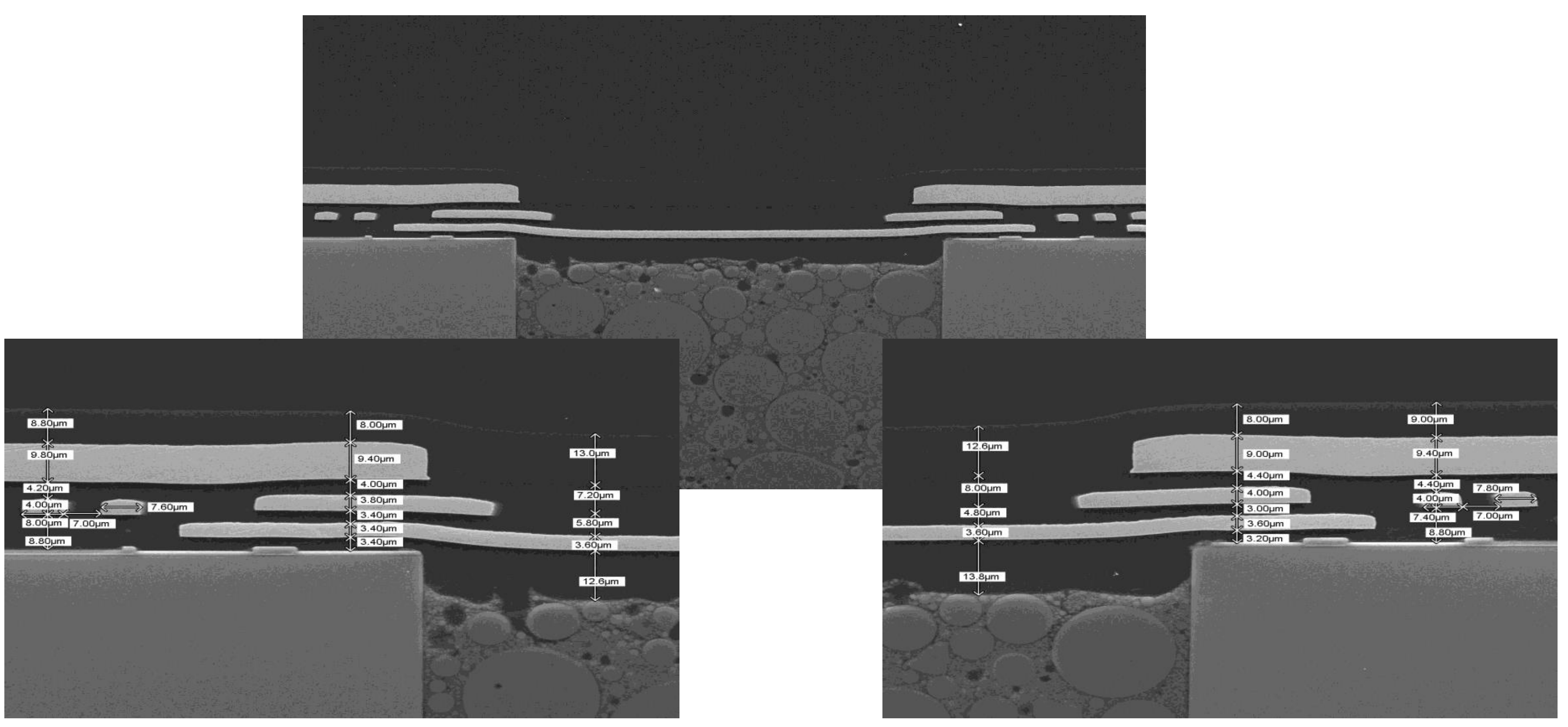
Technology: RDL 1 (2u L/S)







Technology: RDL1 Connection – between Die 1, Die 2



Conclusion

Micro-Electronics Industry: Paradigm Changes

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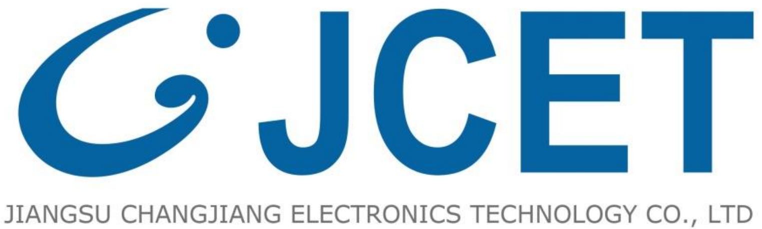
- Heterogeneous Integration is key enabler to solve the next decade's system challenges
- Diverse packaging solutions will provide customers with cost-effective solutions
- Successful product introductions will be facilitated by partnership and collaboration across supply chain partners:
  - OEMs/system houses
  - Design houses
  - Foundries/OSATs
  - Materials suppliers
  - Component vendors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